Engr 233 Electronic CAD Practical work

Week 7

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Operational amplifiers used in oscillators:

Wien bridge sinusoidal oscillator with gain control

Primary Objectives:

- To provide a basic understanding of a particular kind of sinusoidal oscillator circuit.
- To provide an insight into design with non-ideal components.

Introduction: Basics of oscillators:

An oscillator is a circuit that converts a DC input to an AC output. Sinusoidal oscillators consist of an amplification element in a positive feedback loop with a frequency selective network. The amplifier can be a single transistor amplifier or an operational amplifier. The frequency selective network determines the frequency of the oscillator.

The criteria for an oscillator to produce sinusoidal oscillations is that the magnitude of the loop gain is equal to unity and the phase of the loop gain is equal to zero (or multiples of 2π) at the frequency selected for oscillations. This criterion is stated more formally as the Barkhausen criteria, an explanation of which can be found in most good electronics texts.

An oscillator with a loop gain of exactly unity is unrealizable because of varying component values, parameters and temperatures. To keep oscillations from ceasing or increasing, some form of amplitude limiting mechanism can be employed.

In general for a sine wave oscillator such as the Wien (pronounced veen) bridge oscillator, when the circuit is switched on small random perturbations which are always present in a circuit pass round the loop and the frequency component $f = f_o$ (where f_o is the designed oscillation frequency) builds up. This assumes that the loop gain is initially greater than 1. If the build up is not controlled the amplifying device will go into saturation. For an op-amp the peak amplitude of the signal will saturate just below the supply voltages.

Figure 1

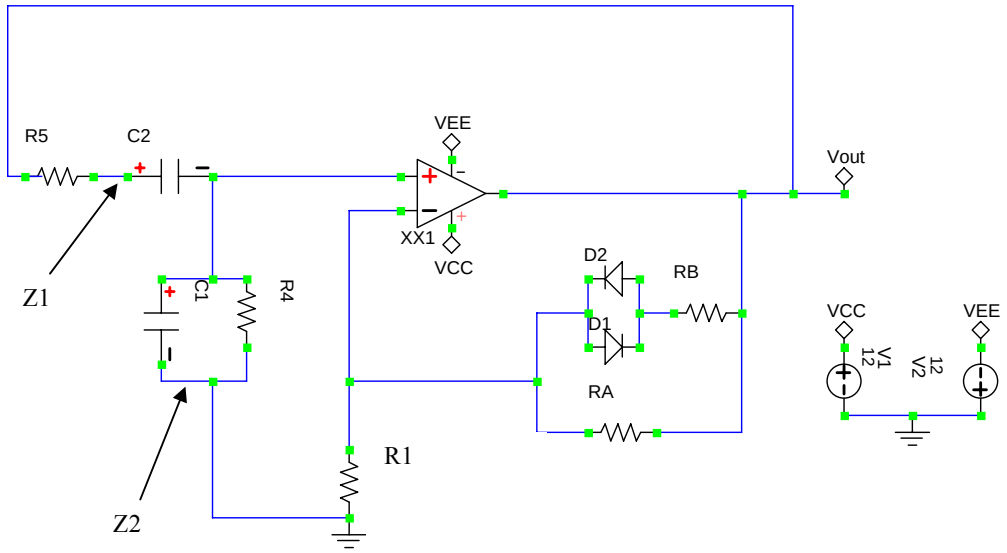

Figure 1: Showing a schematic diagram for a Wien bridge oscillator.

Circuit Diagram, notes and associated equations:

Some notes on circuit features:

The above circuit can be considered in two separate parts as follows:

- **Forward gain setting:** Considering the feed back network consisting of RB, RA, D1, D2 and R2. This network can be compared with the feedback network of the non-inverting amplifier (see week 6) where the combination of RB, D1, D2, and RA is equivalent to R2.
- **Positive feedback frequency selective network:** The network comprises of the components R5, C2, R4, and C1. This network provides positive feedback at a frequency defined by :

  $$f_o = \frac{1}{2\pi RC}$$

  Where R = R5 , R4 and C = C1 and C2.
  It can be shown (or found in relevant texts) that at the oscillation frequency the positive feedback has a zero phase shift and has a gain of 1/3. Therefore for the circuit to oscillate the forward gain network (cf above "forward gain

setting") should have a gain of 3 and introduce a zero phase shift. The zero phase shifts is inherent in the forward path, thus leaving the gain to be set.

- **Diodes D1 and D2:** These provide automatic gain control and stop the oscillator going into saturation. That, is they provide an amplitude limiting mechanism.

Design equations for exercises

For an ideal Opamp.
The above oscillator will oscillate at the frequency:

$$f_0 = \frac{1}{2\pi RC}$$

Where R and C indicate the components in the feedback path from the output to the non-inverting input. That is:
R = R4 and R5
C = C1 and C2

For oscillations to be maintained and to be amplitude controlled we require that:
For oscillation:

$$\frac{RA}{R1} \approx 2$$

Note: to ensure oscillations start the value R2/R1 should be made slightly greater than 2
Hint: a value of around 2.2 should work.
For amplitude control:
We require that:

$$\frac{RA \,||\, RB}{R1} < 2$$

Where RA || RB indicates RA in parallel with RB
Note: To ensure the amplitude is limited correctly the value of the combination above should be made slightly less than 2.
Hint: a value of around 1.8 should work.

Note further equations giving the calculations for the frequency selective network are given on page 5. However, these are not necessary to carry out the exercises.

Exercise 1

Note: For this exercise make sure you use the following components:

OP-Amp:
Toolbar >> Categories >> OPAMP >> uA741 (the third one from the bottom of the list)
Diodes:
Toolbar >> Categories >> Diodes >> 1N4001 (approximately half way down list)

In addition also make sure that you design the circuit using preferred values for components. Details of the preferred values are given on page 6

Enter the schematic of figure 1
Note: there is no need to enter the comments indicating Z1 and Z2.
Using preferred component values design a Wien bridge oscillator with an oscillation frequency of approximately 2kHz.

Hints: You could start by setting R1 to 10k and C1 and C2 to 0.01uF.

Using transient simulations verify the operation of the circuit.
Note: Initially run a transient simulation to view one cycle of the expected output. Then run simulations over a longer time so that complete circuit operation can be determined.

Question 1

a. What is the approximate start up time of the oscillator?
b. State the component values you used for the oscillator.
c. What is the oscillation frequency of the oscillator?

Standard component values may vary between ± 10% of their nominal values. Experiment with the circuit's frequency selective components to see how the frequency is changed. **Hint:** Try using worst-case R's.

Question 2

a. Approximately how much does the frequency vary from the nominal for worst-case resistor values?
b. How could you design the circuit to be tunable?

Now try to design an oscillator with an oscillation frequency of 25Khz and evaluate the circuit using simulations.

Question 3

a. Briefly explain the circuit response and why it may operate as it does.

Frequency selective network calculations

The frequency selective circuit is a potential divider formed by impedances Z_1 and Z_2 Where:

$$Z_1 = R + \frac{1}{j\omega C}$$

and using admittances because Z_2 is a parallel network

$$\frac{1}{Z_2} = \frac{1}{R} + j\omega C$$

After some manipulation this leads to the positive feedback factor β_v

$$\beta_v = \frac{1}{3 + j\left(\omega CR - \frac{1}{\omega CR}\right)}$$

Now the phase shift will go to zero when the imaginary term in the denominator goes to zero. This will occur when:

$$\omega_0 CR - \frac{1}{\omega_0 CR} = 0$$

Which provides the result:

$$\omega_0 = \frac{1}{CR}$$

So at ω_0

$$\beta_v = \frac{1}{3 + j(zero)} = \frac{1}{3}\angle 0$$

so the forward amplifier has to provide a gain of 3 to make the gain around the loop equal to unity. In addition the forward gain must have a zero phase shift. This condition is satisfied because the forward gain is set by a non-inverting amplifier configuration.

Resistor and capacitor preferred values:

resistance values ($\times 10^n$)

10	16	**27**	43	**68**
11	**18**	30	**47**	75
12	20	**33**	51	**82**
13	**22**	36	**56**	91
15	24	**39**	62	**100**

Ceramic-disk capacitors

3.3	30	200	600	2700
5	39	220	680	3000
6	47	240	750	3300
6.8	50	250	800	3900
7.5	51	270	820	4000
8	56	300	910	4300
10	68	330	1000	4700
12	75	350	1200	5000
15	82	360	1300	5600
18	91	390	1500	6800
20	100	400	1600	7500
22	120	470	1800	8200
24	130	500	2000	
25	150	510	2200	
27	180	560	2500	

Tantalum capacitors ($\times 10^n$) (to 330 μF)

0.0047	0.010	0.022
0.0056	0.012	0.027
0.0068	0.015	0.033
0.0082	0.018	0.039

Note: For real components the above values will be subject to a 10% tolerance.

Answer Sheet: Week 7 **Student**

Question 1

a)

b)

c)

Question 2

a)

b)

Question 3

a)